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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,853	08/29/2001	Robert L. Candela	43221-S (MUR 0542 00 US)	7507

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EXAMINER
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GREENE, PERSHELLE L

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/18/2002

Please find below and or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/941,853	CANELLA, ROBERT L
	Examiner	Art Unit
	Pershelle Greene	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 29 August 2001.

2a)  This action is **FINAL**.      2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-65 is/are pending in the application.

4a) Of the above claim(s) 7,9,20,21,23,27-43 and 56-65 is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed

6)  Claim(s) 1-6,8,10-13,15-19,22,25,26 and 44-55 is/are rejected.

7)  Claim(s) 14 and 25 is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.182.

11)  The proposed drawing correction filed on \_\_\_\_\_ is: a)  approved b)  disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.

12)  The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)  Acknowledgment is made of a claim for foreign priority under 35 U S C. § 119(a)-(d) or (f)  
a)  All b)  Some \* c)  None of  
1.  Certified copies of the priority documents have been received  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a))  
\* See the attached detailed Office action for a list of the certified copies not received

14)  Acknowledgment is made of a claim for domestic priority under 35 U S C. § 119(e) (to a provisional application)  
a)  The translation of the foreign language provisional application has been received

15)  Acknowledgment is made of a claim for domestic priority under 35 U S C. §§ 120 and or 121

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-348)  
3)  Information Disclosure Statement(s) (PTO-1449) Paper No/s: 2&3  
4)  Interview Summary (PTO-413) Paper No/s: \_\_\_\_\_  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other \_\_\_\_\_

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Serial Number: 09 941853  
Attorney's Docket #: 4322US (MUEI-0542.00 US)

Filing Date: 8/29/2001

Applicant: Canella, Robert L.  
Examiner: Pershelle Greene

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election without traverse of Species I in Paper No. 11 is acknowledged.

### ***Drawings***

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second layer of resilient conductive material must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Specification***

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 13 and 26 are being rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 13, claim 13 refers to "said surface", it is unclear what surface to which you are referring. Claim 13 depends from claim 5 in which the applicant refers to "at least one of said first and second surfaces". Where is there a mention of "said surface". Are you referring to a first or second surface?

As to claim 26, claim 26 refers to "a second layer of resilient conductive material", it is unclear where this is shown in the drawings. Is there a second layer of resilient conductive material and if so, where?

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States

7. Claims 1-6, 8, 10-11, 13 and 4-52 are being rejected under 35 U.S.C. 102(b) as being anticipated by Grabbe (U.S. Patent # 5,173,055).

As to claim 1, Grabbe discloses an area array connector having all of the claimed subject matter:

- A. "a substrate" is met by the substrate 40 shown in figure 8;
- B. "a layer of resilient conductive material ... integrated circuit device" is met by the layer of resilient conductive material 18 disposed on a surface of the substrate 40.

The conductive layer defines a plurality of electrically isolated spring-biased electrical contacts 18. Each of the electrically isolated spring-biased electrical contacts having an electrically isolated conductive trace extending therefrom and including a surface configured for biasing against and electrically contacting a lead element of an integrated circuit device shown in figure 9.

As to claim 3, Grabbe discloses an area array connector having all of the claimed subject matter:

- A. "a substrate" is met by the substrate 40 shown in figure 8;
- B. "a layer of resilient conductive material ... integrated circuit device" is met by the layer of resilient conductive material 18 disposed on a surface of the substrate 40. The conductive layer defines a plurality of electrically isolated spring-biased electrical contacts 18. Each of the electrically isolated spring-biased electrical contacts having an electrically isolated conductive trace extending therefrom and including a surface configured for biasing against and electrically contacting a lead element of an integrated circuit device shown in figure 9.

As to claim 3, Grabbe discloses an area array connector having all of the claimed subject matter:

- A. "a substrate ... surface" is met by the substrate 40 shown in figure 8;
- B. "a layer of resilient conductive material ... of said substrate" is met by the layer of resilient conductive material 18 having at least one portion of the substrate. Refer to figure 8;
- C. "at least one spring-biased electrical contact ... an integrated circuit device" is met by the spring-biased electrical contact 18 formed in the layer of resilient conductive material and electrically isolated from the layer of resilient conductive material by an aperture that is formed in the layer of resilient conductive material. At least one of the spring-biased electrical contacts includes a surface configured for biasing against and electrically contacting a lead element extending from an integrated circuit device; and
- D. "at least one conductive trace ... spring biased electrical contact" is met by the conductive trace formed in the layer of resilient conductive material 18 and electrically isolated from the layer of resilient conductive material y at least on cavity (the area under the spring is the cavity). At least one conductive trace terminates at one of the spring-biased electrical contacts. Refer to figure to figures 8 and 9.

As to claims 2, 4, and 6, Grabbe shows, in figure 9, a plurality of vias 46 under the spring-biased electrical contact extending through the substrate.

As to claims 8, 10, 11, and 13, Grabbe shows, in figure 9, a cantilevered spring 18 having a permanent deflection. The resilient conductive material comprises a laminate bonded to one of the surfaces of the substrate. The spring-biased electrical contact includes at least one contact element disposed on the surface of the substrate which is configured to remove or puncture through a layer of contaminants.

As to claims 44-52, Grabbe shows, referring to figure 9, a dielectric layer of sufficient thickness overlying the layer of resilient conductive material and having apertures aligned with the electrically isolated spring-biased electrical contacts. The apertures are of a frustoconical configuration.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 15-19, 22, 24, 26, and 53-55 are being rejected under 35 U.S.C. 103(a) as being unpatentable over Grabbe (U.S. Patent # 5,173,055) in view of McMillan et al. (U.S. Patent 5,829,988).

In claims 15 and 26, in so far as can be understood, Grabbe shows, in figure 9, a substrate having a first and second surface. There is a layer of resilient conductive material 18 disposed on the first surface of the substrate. Pluralities of spring-biased electrical contacts are formed in

the layer of resilient conductive material. Each spring is isolated from the layer of resilient conductive material by an aperture in the layer of resilient conductive material. Pluralities of traces are formed in the layer of resilient conductive material. At least a portion of the plurality of traces terminates at the spring-biased electrical contact. Each trace is electrically isolated from the layer of resilient conductive material and all other traces by the cavity (the area under the spring-biased electrical contact). Grabbe fails to explicitly show an integrated circuit device disposed on the first surface of the substrate.

McMillan et al. is cited for showing a socket assembly for integrated circuit chip carrier package. Specifically McMillan shows, referring to figure 3A, an integrated circuit device disposed on a first surface of a substrate.

As to claim 16, McMillan shows, in figure 3A, a clamping device 16.

It would have been obvious to one of ordinary skill in the art to use the integrated circuit of McMillan with the device of Grabbe for the purpose of performance enhancement. The clamping feature aids in holding the components together more tightly.

As to claims 17-19, 22 and 24, Grabbe shows, referring to figure 9, a cantilevered spring-biased electrical contact configured to remove or puncture through a layer of contaminants formed on a surface of a mating lead that includes a permanent deflection away from the surface of the substrate. There is a plurality of vias disposed in the substrate. Each of the vias is positioned at a location underlying the spring biased electrical contact.

As to claims 53-55, Grabbe shows, referring to figure 9, a dielectric layer of sufficient thickness overlying the layer of resilient conductive material and having apertures aligned with

the electrically isolated spring-biased electrical contacts. The apertures are of a frustoconical configuration.

10. Claim 12 is **product-by-process claim**.

#### *Claim Objections*

11. Claims 14 and 25 are being objected to as being dependent upon a rejected base claim.

#### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pershelle Greene whose telephone number is 703-305-3870. The examiner can normally be reached on M-F 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

PLG  
December 16, 2002

Supervisory  
Patent Examiner  
PLG



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